at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells.

8. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a second address decoder operatively coupled to the at least one common line, the second address decoder configured to receive an input address and select one or more common lines.

10. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a reference generator coupled to the at least one memory decoder and the reference array, the reference generator configured to provide a first set of signals to the reference array and the bias signals to the at least one memory decoder.

16. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

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a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells,

wherein each memory array includes a plurality of segments, each segment including P rows by Q columns of memory cells.

21. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

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at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a plurality of current sinks disposed along each of the at least one common line.

28. (amended) A data storage system comprising:

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a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

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a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells,

wherein each common line is driven from both sides of a memory array.

30. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

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at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells,

wherein the reference cells are disposed at approximately linearly spaced locations along the at least one common line.

31. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells,

wherein the reference cells are disposed at approximately geometrically spaced locations along the at least one common line.

32. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells, each reference array includes a plurality of reference cells, each reference cell operative to provide one reference signal; and

a plurality of reference lines coupled to the plurality of reference cells, wherein resistance of the reference lines is approximately matched to resistance of common lines.

34. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

wherein the reference array includes a plurality of reference cells, each reference cell hhoperative to provide one reference signal,

wherein each reference signal is generated by averaging outputs from two or more reference cells.

35. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

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the reference array includes a plurality of reference cells operative to provide the reference signals, wherein at least one of the reference signals is generated by extrapolating outputs from two reference cells.

43. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

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a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a plurality of drivers coupled to the plurality of bit lines, each driver configured to control an associated bit line during write, read, or erase operation,

each driver comprising a voltage comparator coupled to the associated bit line and a reference source, the voltage comparator configured to compare a voltage on the bit line and one of the reference signals from the reference array and to provide a comparison result,

wherein each driver further comprises:

a multiplexer operative to receive the reference signals from the reference array and to provide one of the reference signals to the voltage comparator.

44. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a plurality of drivers coupled to the plurality of bit lines, each driver configured to control an associated bit line during write, read, or erase operation,

wherein each driver is associated with one memory cell during programming, and wherein each driver further comprises: an inhibit circuit operative to enable or inhibit programming of a particular memory cell coupled to the associated bit line.

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45. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

cont.

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a plurality of drivers coupled to the plurality of bit lines, each driver configured to control an associated bit line during write, read, or erase operation,

wherein each driver is associated with one memory cell during programming, and

wherein each driver further comprises:

control circuitry configured to generate a first status signal indicative of a particular memory cell coupled to the associated bit line being placed in a program inhibit mode.

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49. (amended) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

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a plurality of drivers coupled to the plurality of bit lines, each driver configured to control an associated bit line during write, read, or erase operation,

cont.

wherein each driver includes control circuitry configured to generate a third status signal indicative of a particular memory cell coupled to the associated bit line being incompletely programmed.

Please add new claims 54-83 as follows:

54. (new) The system of claim 8, wherein the reference array comprises a plurality of reference cells, and wherein the reference cells and memory cells selected for programming are biased with approximately similar bias conditions on their control gates, control lines, and bitlines.

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55. (new) The system of claim 54, wherein the each set of reference cell and associate memory cell shares the same common line and control gate line.

56. (new) The system of claim 8, further comprising:

a first address decoder operatively coupled to the plurality of bitlines, the first address decoder configured to receive an input address and select one or more bitlines.

57. (new) The system of claim 8, further comprising:

a third address decoder operatively coupled to the plurality of control gate lines, the third address decoder configured to receive an input address and select one or more control gate lines.

58. (new) The system of claim 8, wherein the reference array includes

a plurality of reference cells, each reference cell operative to provide one reference signal.

59. (new) The system of claim 8, wherein the reference signals define 2^N unique levels used for programming and reading the memory cells.

60. (new) The system of claim 8, wherein the reference signals define 2^N-1 unique levels used for programming and reading the memory cells.

61. (new) The system of claim 60, wherein the reference cells are programmed with a set of reference values.

62. (new) The system of claim 61, wherein reference cells previously programmed are inhibited from further programming.

63. (new) The system of claim 8, further comprising:

a plurality of drivers coupled to the plurality of bit lines, each driver configured to control an associated bit line during write, read, or erase operation.

64. (new) The system of claim 63, wherein each driver comprises:

a plurality of N data latches configured to receive and latch N data bits from a memory cell during a read operation.

65. (new) The system of claim 63, wherein each driver further comprises:

a voltage comparator coupled to the associated bit line and a reference source, the voltage comparator configured to compare a voltage on the bit line and one of the reference signals from the reference array and to provide a comparison result.

66. (new) The system of claim 63, wherein the plurality of drivers are configured to generate a second status signal indicative of all memory cells associated with the plurality of drivers being placed in the program inhibit mode.

67. (new) The system of claim 8, wherein voltages for memory cells not selected for programming are set to approximately zero.

68. (new) The system of claim 10, wherein the reference array comprises a plurality of reference cells, and wherein the reference cells and memory cells selected for programming are biased with approximately similar bias conditions on their control gates, control lines, and bitlines.

69. (new) The system of claim 68, wherein the each set of reference cell and associate memory cell shares the same common line and control gate line.

70. (new) The system of claim 68, further comprising:

a first address decoder operatively coupled to the plurality of bitlines, the first address decoder configured to receive an input address and select one or more bitlines.

71. (new) The system of claim 10, further comprising:

a third address decoder operatively coupled to the plurality of control gate lines, the third address decoder configured to receive an input address and select one or more control gate lines.

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72. (new) The system of claim 10, wherein the reference array includes

a plurality of reference cells, each reference cell operative to provide one reference signal.

73. (new) The system of claim 10, wherein the reference signals define 2^N unique levels used for programming and reading the memory cells.

74. (new) The system of claim 10, wherein the reference signals define 2^N-1 unique levels used for programming and reading the memory cells.

75. (new) The system of claim 68, wherein the reference cells are programmed with a set of reference values.

76. (new) The system of claim 75, wherein reference cells previously programmed are inhibited from further programming.

77. (new) The system of claim 10, further comprising:

a plurality of drivers coupled to the plurality of bit lines, each driver configured to control an associated bit line during write, read, or erase operation.

78. (new) The system of claim 77, wherein each driver comprises:

a plurality of N data latches configured to receive and latch N data bits from a memory cell during a read operation.

79. (new) The system of claim 77, wherein each driver further comprises:

a voltage comparator coupled to the associated bit line and a reference source, the voltage comparator configured to compare a voltage on the bit line and one of the reference signals from the reference array and to provide a comparison result.

B 11 cont.

80. (new) The system of claim 77, wherein the plurality of drivers are configured to generate a second status signal indicative of all memory cells associated with the plurality of drivers being placed in the program inhibit mode.

81. (new) The system of claim 10, wherein voltages for memory cells not selected for programming are set to approximately zero.

82. (new) A data storage system comprising:

a plurality of segmented memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells.

83. (new) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to said at least one common line to select ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells.

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